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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/661,562 | 09/15/2003 | Hsiao-Ping Chu | CHUH3003/EM | 1802 |

23364 7590 03/15/2005

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| EXAMINER | |
|---|---|
| NGUYEN, JOSEPH H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2815 | |

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/661,562 | CHU, HSIAO-PING | |
| | Examiner | Art Unit | |
| | Joseph Nguyen | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *9/15/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 3, it is not understood what applicant regards as "a plurality of first insulation layers in the first and the second groves" since a plurality of first insulation layers formed on the diodes at the first surface of the semiconductor wafer is also cited in claim 1 from which claim 3 depends, and whether this so called plurality of first insulation layers are new elements or the cited element in claim 1 is not clear.

Claims 4-8 are also rejected due to its dependence upon the rejected base claim 3 above.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Chen et al. discloses on figure 13a a chip diode for surface mounting comprising a first type semiconductor 11 having a predetermined depth formed on a first surface of a semiconductor wafer by diffusion; a second type semiconductor 10 having a predetermined depth formed on a second surface of a semiconductor wafer by diffusion wherein the second type semiconductor is different from the first type semiconductor and the second surface is opposite the first surface; a plurality of diodes formed on each of the first and the second surfaces of the semiconductor wafer (col. 3, lines 15-38); a plurality of first insulation layers 35 formed on the diodes at the first surface of the semiconductor wafer for diving the semiconductor wafer into two separated and insulated portions; a plurality of first conductive metal layers 13 coated on a central portion of the semiconductor wafer as a first conductive terminal for soldering; and a plurality of second conductive metal layers 41 on an edge of the semiconductor wafer and extended to sides of the second type

semiconductor on the second surface of the semiconductor wafer to be in communication therewith as a second conductive terminal for soldering.

Regarding claim 2, Chen et al. discloses on figure 13a at least one layer 41 of conductive metal on a first surface of the diodes corresponding to a central portion of the semiconductor wafer. Note that the phrase "each of the first and the second conductive metal layers is formed by chemically plating" is merely product by process and therefore does not structurally distinguish from Chen et al.

Regarding claim 3, as best understood, Chen et al. discloses on figures 9 and 13a a plurality of parallel, spaced first grooves 32 and second grooves 33 formed on the first type semiconductor at the first surface of the diodes along X and Y axes, each of the first grooves and the second grooves being penetrated through the first type semiconductor into the second type semiconductor formed by sintering (col. 5, lines 1-2); and a plurality of first insulation layers 35 in the first and the second grooves, the first insulation layers being adapted to separate and insulate the first type semiconductor from the second type semiconductor at both sides.

Regarding claim 4, Chen et al. discloses on figure 13a the first insulation layers are glass insulation layers formed by sintering glass plasma (col. 5, lines 1-40).

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If

attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
March 7, 2005

ALLAN R. WILSON
PRIMARY EXAMINER